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09/705,050	11/02/2000	Masahiko Nakayama	P/1866-54	3890

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EXAMINER
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ART UNIT	PAPER NUMBER
2124	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/705,050	NAKAYAMA, MASAHIKO	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This communication is responsive to Amendment A, filed 12/3/2003.

2. Claims 2-21 are pending in this application. Claims 2, 10, and 17 are independent claims. In the Amendment A, claim 1 is cancelled, claims 2-9 are amended, and claims 10-21 are newly added. This action is made final.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations cited in dependent claims as "the control means is constituted by a second n-bit shift register for shifting a ram-up/down signal through successive bit stages under control of a shift clock for the first n-bit shift register" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 2, 10, and 17 are objected to because of the following informalities: the applicant is advised to replace the term "FIR" as "Finite Impulse Response (FIR)" once for every independent claims. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 4 and 17-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 4, the limitation "the basis" in line 3 lacks an antecedence basis. For examination purposes, the examiner considers this limitation as "a basis".

Re claim 17, the limitation "the FIR filter coefficient circuits" in claim is unclear whether the limitation is referring to the coefficient circuits as {h1...hn} or the input data {d1...dn}. For examination purposes, the examiner considers this limitation as the input data {d1...dn}.

Thus, claims 18-21 are also rejected for being dependent on the rejected base claim 17.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 2, 4-7, 10, 14, 16-17, 19, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Hidemitsu (J.P. 411088119A).

Re claim 2, Hidemitsu discloses in Figure 7 an FIR filter comprising: a selection control means (1-10, 22, and 24-28) for selecting input data (IN), the selection control means including: a first n-bit shift register (n being a natural number n = 5 as x[1]...x[5]) for progressively shifting the input data through successive stage bits (the data "IN" is shifting to the right into the register), n switching means (6-10) respectively provided for the outputs of the n stage bits of the n-bit shift register (inputs into 11-15), respectively, for controlling the outputs of these n bits, and a control means (22) for controlling the n switching means (6-10) the control means outputting n unique control signals respectively to the n switching means (S1-S5); and a multiplying means (11-15) for multiplying data selected by the selection control means (1-10, 22, and 24-28) and a predetermined filter coefficient (16-20), wherein a FIR filter output (23 as OUT) is derived from the product outputs of the multiplying means.

Re claim 4, Hidemitsu further discloses in Figures 7 and 11 the control means (Figure 11) is a second n-bit shift register (108-113) for shifting a ramp-up/-down signal on the basis of the shift clock signal (T1) of the first n-bit shift register (Figure 7 parts 2-5); and the n switching means (6-10) are n switches provided for the bit stages of the second n bit shift register (S1-S5) for selectively feeding out the filter coefficient data and zero data on the basis of the outputs of the corresponding bit stages (Figure 1).

Re claim 5, Hidemitsu further discloses in Figures 7 and 11 the control means (Figure 11) is a second n-bit shift register (108-113) for shifting a ramp-up/-down signal

through the successive bit stages under control of a shift clock signal (T1) for the first n-bit shift register, the wherein outputs of the bit stages of the first n- bit shift register are reset on the basis of the outputs of the corresponding bit stage of the second n-bit shift register (Figure 1).

Re claim 6, Hidemitsu further discloses in Figure 11 a means for changing a shift clock frequency (105) of the first n-bit shift registers.

Re claim 7, Hidemitsu further discloses in Figure 11 the control means (Figure 11) includes a second n-bit shift (108-113), wherein the shifting operation of the first and second n-bit shift registers are operated under control of shift clock signals at different frequencies (T1 and shift-in of IN frequency).

Re claim 10, it has the similar features cited in claim 1. Thus, claim 10 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 14, Hidemitsu further discloses in Figure 11 the control circuit includes a second n-bit shift register (108-113).

Re claim 16, it has the same limitations cited in claim 7. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 17, Hidemitsu further an FIR filter in Figures 1, 7, and 11 comprising: a first n-bit shift register (Figure 7 parts 24-28) that receives an input signal (IN part 1) and outputs a first-register output signal (output of D registers); a control circuit that outputs n unique control signals (S1-S5); n switching circuits (6-10), each switching circuit (Figure 1) comprising: circuit for producing a fixed value ("0"); circuit for producing a FIR filter coefficient (input data from n-registers); switch coupled to the control circuit

(22), coupled to the fixed value circuit and coupled to the FIR filter coefficient circuit, each switch selecting either the fixed value or the FIR filter coefficient depending upon the control circuit output signal, outputting a switch selection output; multiplier (11-15) coupled to the switch and coupled to the first n-bit shift register, the multiplier multiplying the switch selection output with a selected one of the n first-register output signals to produce a switching circuit output; and an adder (21)coupled to the n switching circuits, the adder adding the outputs of the n switching circuits (23).

Re claim 19, Hidemitsu further discloses in Figure 11 the control circuit includes a second n-bit shift register (108-113).

Re claim 21, it has the same limitations cited in claim 7. Thus, claim 21 is also rejected under the same rationale in the rejection of rejected claim 7.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3 and 11-12 are rejected under 35 U.S.C. 103(a) as being obvious over Hidemitsu (J.P. 411088119A), as applied to claim 2 above, in view of Shinde (U.S. 6,192,386).

Re claim 3, Hidemitsu discloses in Figure 11 the control means (Figure 11) is constituted by a second n-bit shift register (108-110) for shifting a ramp-up/-down signal through the successive bit stages under control of a shift clock for the first n-bit shift

register (T1). Hidemitsu does not disclose the n switch means are each an AND gate for receiving the outputs of the corresponding bit stages of the first and second n-bit shift registers as respective inputs. However, Shinde discloses in Figures 9 and 11 that the switch means (Figure 9 part 1) is constituted by an AND gate (Figure 11 part 221-228) for receiving the outputs of the corresponding bit stages of the first (input Y from 211-214) and second n-bit shift registers (CLK2) as respective inputs. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a concept of an AND gate utilizing in switch means for receiving the output of the corresponding bits stages of the first and second n-bit shift registers as respective inputs as seen in Shinde's invention Figure 11 into Hidemitsu's invention because it would enable to simplify the circuitry and to reduce the power consumption by the switches.

Re claims 11-12, they have similar features cited in claim 3. Thus, claims 11-12 are also rejected under the same rationale in the rejection of rejected claim 3.

11. Claims 8-9, 13, 15, 18, and 20 are rejected under 35 U.S.C. 103(a) as being obvious over Hidemitsu (J.P. 411088119A) in view of Shinde (U.S. 6,192,386) and in further view of the admitted prior art.

Re claims 8-9, Hidemitsu in view of Shinde discloses an adder circuit for adding together the outputs of the n multiplying circuits (Figure 7 part 21). Hidemitsu in view of Shinde does not disclose a ramp-up/down signal is fed to the first n-bit shift register, the ramp-up data being derived from the sum output of the adder circuit. However, the

admitted prior art discloses in pages 6-7 that the ramp-up/down data being derived from the sum output of the adder circuit (lines 1-5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the ramp-up/down data being derived from the sum output of the adder circuit as described in the admitted prior art into Hidemitsu in view of Shinde's invention because it enable to reduce the computation for efficiently controlling power signal.

Re claims 13, 15, 18, and 20, they have similar features cited in claims 8-9. Thus, claims 13, 15, 18, and 20 are also rejected under the same rationale in the rejection of rejected claims 8-9.

Response to Arguments

12. Applicant's arguments with respect to claims 2-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

February 2, 2004

TODD INGBERG
PRIMARY EXAMINER